A Study of MIMIM On-Chip Capacitor Using Cu/SiO_2 Interconnect Technology

Chen Zhen, Guo Lihui, Yu Mingbin, and Zhang Yi

***Abstract*—In this work, metal–insulator–metal–insulator–metal (MIMIM) on-chip capacitor is fabricated newly using Cu/SiO_2 backend technology. Capacitance density 1.7 fF/μm^2 has been achieved with satisfactory dc and RF characteristics. Compared with conventional metal–insulator–metal (MIM) capacitor, MIMIM doubles the capacitance density without weakening capacitor's quality in both dc and RF characteristics. And, its yield is predictable. Therefore, it has been approved to be a convenient and reliable method to improve capacitance density for on-chip standard Cu/SiO_2 backend technology.**

***Index Terms*—Capacitors, CMOS integrated circuits, interconnections, metal-insulator-metal devices, very-high-frequency devices, yield estimation.**

I. Introduction

METAL–INSULATOR–METAL (MIM) capacitor is frequently applied in monolithic RF and microwave integrated circuit. In order to keep up with the reduction of chip size, researches on increasing capacitance density have never stopped. Multilayer capacitor, as a method to increase capacitor density, has been studied by previous researches [1], [2]. But, in standard Cu/SiO_2 interconnect technology, it has never been applied. The reason might be to avoid more processing steps, compared with conventional MIM capacitor. Conventionally, there are two ways that researchers explored to achieve high capacitance density for on-chip capacitor. One is applying capacitor dielectric with higher K value. SiO_2 was initially studied [3] and then was replaced by Si_3N_4. Recently, many researches try to introduce high K materials such as Ta_2O_5 to be capacitor dielectric. The other is to make the capacitor dielectric thinner. For example, when Si_3N_4 started to be applied, the typical thickness was 2000 Å [4]. After that, thinner and thinner Si_3N_4 layer was studied. In 1999, J.-H. Lee *et al.* tried ultrathin (200 Å) Si_3N_4 to increase capacitance density to 2.9 fF/μm^2 [4]. But, correspondingly, there shows up parasitic factors, especially dc characteristics, which is the main challenge. For example, in Jae-Hak Lee's study, the breakdown voltage decreased to 6–18 V [2].

This work is based on the platform of 0.18 μm Cu/SiO_2 interconnect technology. MIM capacitor with 700 Å Si_3N_4 (capacitance density 0.85 fF/μm^2) had been previously achieved as baseline. MIMIM on-chip capacitor was fabricated without changing Si_3N_4 thickness. This is also, to our knowledge, the first time that metal–insulator–metal–insulator–metal (MIMIM) on-chip capacitor is realized using standard Cu/SiO_2 interconnect technology. Capacitance density of 1.7 fF/μm^2 has been achieved with excellent dc and RF characteristics.

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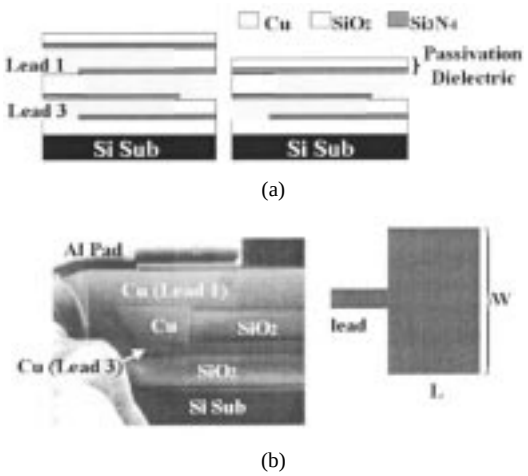

Fig. 1. (a) Schematic MIMIM capacitor; (b) schematic conventional MIM capacitor; (c) FIB image of MIMIM; (d) definition of parameters L, W.

It is true that the processing steps will be more for MIMIM, but, in our work, the additional cost has been approved to be worthy, compared with other ways to improve capacitance density. The reasons will be discussed in detail.

II. Experiment and Characterization

Unlike other solutions to improve capacitance density such as high K dielectric or thinner dielectric, MIMIM capacitor could be fabricated without any process development. Conventional MIM capacitor fabrication procedure based on 0.18 μm Cu backend technology, which has been previously studied [5], [6] could be applied directly.

Fig. 1 illustrates that MIMIM structure is basically placing an additional Si_3N_4/Cu structure on top of conventional MIM capacitor, which is still compatible with standard backend process. Moreover, if all the passive components are integrated, at the top-most added layer, stack spiral inductor can be fabricated to achieve high Q value, which might be an additional reason why more processing steps are worthy. In fact, in Fig. 1(c), the second and third Cu layers are so thick because the capacitor is integrated with spiral inductor. If it is applied in other integration scheme, such thick capacitor metal plate might not be necessary.

Fig. 2 shows capacitance versus capacitor area. In the linear fitting slopes, calculated capacitance densities are 0.85 fF/μm^2 for MIM structure and 1.7 fF/μm^2 for MIMIM structure.

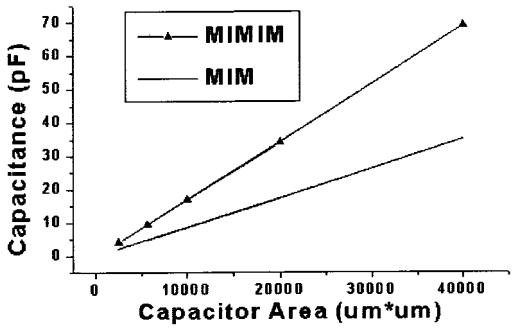

Fig. 2. Comparison of capacitance versus capacitor area (measured at 1 kHz).

Process stability could be illustrated by the excellent linearity of these lines.

Yield is a very important concern. In our study, yields of a selected capacitor (capacitor area: 10 000 μm^2) of MIM with 700 Å Si3N4, MIMIM with 700 Å Si3N4, and MIM with 300 Å Si_3N_4 are 95%, 93% and 55%, respectively. The yield of MIM with 300 Å Si_3N_4 is much lower than the other two because the deposition process is not optimized since it only reduces the deposition time.

In fact, the yield of MIMIM capacitor can be estimated from that of the MIM capacitor with the same fabrication technology. From Fig. 1, it is noticed that MIMIM capacitor can be treated as two parallel-connected MIM capacitors, so the yield condition of MIMIM capacitor is that both of the two MIM capacitors yield. Since the same technology is applied, we assume that the two MIM capacitors obey the same probability distribution of yield. Therefore, at a certain point, if an MIM capacitor's yield probability is P ($P \leq 1$), an MIMIM capacitor's yield probability will be P^2. If a large amount of wafers are investigated to deduce yield probability density function, which is defined as

$$\iint f(x, y)\, dx\, dy = Y_{\mathrm{MIM}} \tag{1}$$

where $f(x, y)$ is the yield probability density at point (x, y) and Y_{MIM} is the total yield of MIM capacitor [7], it can be concluded that

$$Y_{\mathrm{MIMIM}} = \iint [f(x, y)]^2\, dx\, dy. \tag{2}$$

Practically, discrete probability distribution is applied. We measure m selected points on each wafer and find the yield probabilities are $p(1), p(2), \ldots, p(m)$, respectively

$$[p(1) + \cdots + p(m)]/m = Y_{\mathrm{MIM}}. \tag{3}$$

It can be deduced that

$$Y_{\mathrm{MIMIM}} = [p(1)^2 + \cdots + p(m)^2]/m. \tag{4}$$

Therefore, compared with other approaches to improve the capacitance density, MIMIM structure has the advantages of its yield being predictable.

Breakdown is another important concern. Table I shows the comparison of breakdown voltages and breakdown field strength comparison. HP 4156A is applied to measure I–V curve. It is noticed that in Table I, some devices' breakdown voltage is recorded as ">40," since 40 V is the dc bias limitation of the equipment. From the datasheet, it can be found that MIMIM structure shares the same breakdown voltage as MIM structure with the same area and capacitor dielectric type and thickness.

TABLE I
COMPARISON OF BREAKDOWN VOLTAGE AND BREAKDOWN FIELD STRENGTH

Wafer Split	Capacitor size (um^2)	Breakdown Voltage (V)	Breakdown Field Strength (MV/cm)
MIM, 700 Å	2500	>40	>5.7
	10000	>40	>5.7
	100000	30	4.3
MIMIM, 700 Å	2500	>40	>5.7
	10000	>40	>5.7
	100000	31	4.4

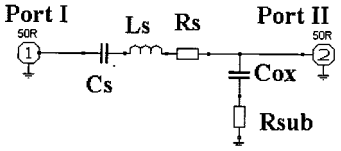

Fig. 3. Equivalent circuit model for MIM and MIMIM capacitor.

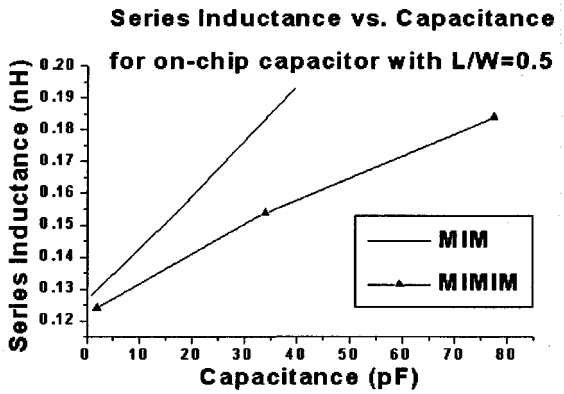

Fig. 4. Series inductance versus capacitance for on-chip capacitor with $L/W = 0.5$.

HP 8510C network analyzer was applied to perform RF characterization. Unlike Ceramic multilayer capacitor (CMC) [2], it is not necessary to develop special equivalent circuit model for MIMIM on chip capacitor. Fig. 3 shows a simple and efficient MIM capacitor equivalent circuit model which is also suitable for an MIMIM capacitor. In this model, Cs, Ls, Rs are series capacitance, inductance, and resistance, respectively, while Cox and $Rsub$ represent the effect of SiO_2 layer and substrate. In this study, our characterized capacitors are inclusive of capacitor leads since leads are necessary for capacitor in IC design and, in this way, we do not need to consider the impact of capacitor leads in our further study.

From Table II, it is noticed that when MIMIM capacitor is applied, at the same layout, series inductance will not be larger than that of MIM capacitor. All the other capacitors with different sizes obtain the same conclusion. On the contrary, as Fig. 4 shows, if we simply increase MIM capacitor area to obtain higher capacitance by keeping the same length/width ratio

TABLE II
EXTRACTED LUMPED ELEMENT COMPARISON (CAPACITOR SIZE: 25 × 50 μm^2, VALID FROM 0.5 GHz TO 10 GHz)

	Cs (pF)	Ls (nH)	Rs (Ω)	Cox (fF)	Rsub (kΩ)
MIM	1.02	0.128	0.61	7.01	4.50
MIMIM	1.91	0.124	0.36	8.49	4.03

[L/W in Fig. 1(d)], the series inductance will also increase. Fig. 4 also illustrates that when comparing with conventional MIM capacitor with the same capacitance, L/W ratio and dielectric type and thickness, MIMIM capacitor will have lower series inductance and, consequently, higher resonant frequency (F_res) since

$$F\_res = 1/(2\pi\sqrt{LsCs}). \tag{5}$$

III. CONCLUSION

MIMIM on-chip capacitor has been fabricated to achieve higher capacitance density. As far as we know, it is also the first time that MIMIM on-chip capacitor is fabricated using standard Cu/SiO_2 interconnect technology. Capacitance density up to 1.7 fF/μm^2 has been achieved. MIM capacitor's equivalent circuit model can be directly applied to analyze MIMIM capacitor.

The processing steps for MIMIM capacitor will be more than that for conventional MIM capacitor, but MIMIM capacitor is still worthy because

1) Technique compatibility: MIMIM on-chip capacitor can be fabricated directly using tolerant technology, not necessary to develop new recipe or even new materials. Before fabrication, the capacitance and yield of MIMIM capacitor can be estimated based on MIM capacitor with the same technology. A method to estimate MIMIM capacitor yield is introduced in this paper.
2) Good dc characteristics: Compared with MIM structure with the same layout and same capacitor dielectric thickness, MIMIM structure has the same breakdown voltage. Unlike high K dielectric or thin dielectric method, it might not be necessary to develop special recipe to enhance reliability of capacitor. Moreover, even a high K dielectric or thinner dielectric process is proved to be qualified, it can be immediately applied associated with MIMIM to double the capacitance density without additional concern of dc characteristics.
3) Good RF characteristics: RF characterization shows that high capacitance density can be achieved by MIMIM without increasing series inductance. Compared with the conventional MIM capacitor with the same capacitance, L/W ratio and dielectric type and thickness, MIMIM capacitor has lower series inductance and higher resonant frequency.

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